Claims

What is claimed is:

1. A computing device comprising:

a clock circuit for generating a first clock signal and a second clock signal;

a first sub functional block (SFB) having an input port for receiving the first clock signal;

a first functional circuit block (FCB) including the first SFB and for operating in accordance with predetermined parameters, the first FCB having a clock control port for providing a first clock control signal and a first clock signal input port for receiving a switchably coupled second clock signal, the first FCB having a circuitry portion for operating in one of a normal mode of operation and in a reduced power consumption mode of operation in dependence upon the switchably coupled second clock signal; and,

a first clock control circuit for receiving the second clock signal and for switchably coupling the second clock signal to the first clock signal input port in dependence upon the first clock control signal.

2. A computing device according to claim 1, wherein the clock circuit is for generating a third clock signal and the computing device comprises:

a second sub functional block (SFB) having an input port for receiving the first clock signal; and,

a second functional circuit block (FCB) including the second SFB and for operating in accordance with predetermined parameters, the second FCB having a second clock control port for providing a second clock control signal and a second clock signal input port for receiving a switchably coupled third clock signal, the second FCB having a circuitry portion for operating in one of a normal mode of operation and in a reduced power consumption mode of operation in dependence upon the switchably coupled third clock signal.

3. A computing device according to claim 2, comprising a second clock control circuit for receiving the third clock signal and for switchably coupling the third clock signal to the second clock signal input port in dependence upon the second clock control signal.

4. A computing device according to claim 2, wherein the first FCB comprises a first FCB control input port and a first FCB control output port, and where the second FCB comprises a second FCB control input port and a second FCB control output port, the first FCB control output port coupled to the second FCB control input port for receiving a FCB control signal from the first FCB for enabling and disabling of the second FCB circuitry portion.

5. A computing device according to claim 2, wherein the first FCB comprises a first FCB control input port and a first FCB control output port, and where the second FCB comprises a second FCB control input port and a second FCB control output port, the second FCB control output port coupled to the first FCB control input port for receiving a FCB control signal from the second FCB for enabling and disabling of the first FCB circuitry portion.

6. A computing device according to claim 1, wherein a plurality of power consumption modes of operation for the first FCB are achievable between the normal mode of operation and the reduced power consumption mode of operation.

7. A computing device according to claim 2, wherein a plurality of power consumption modes of operation for the second FCB are achievable between normal mode of operation and the reduced power consumption mode of operation.

8. A computing device according to claim 1, comprising a frequency multiplier and divider circuit coupled with the clock circuit for receiving of at least one of the first clock signal and the second clock signal for varying a frequency of at least one of the first clock signal and the second clock signal.

9. A computing device according to claim 1, comprising a frequency multiplier and divider circuit coupled with the first functional circuit block (FCB) the clock circuit for decreasing a frequency of the first clock signal when the first FCB is for operating in the reduced power consumption mode of operation.

10. A computing device according to claim 1, comprising a frequency multiplier and divider circuit coupled with the first functional circuit block (FCB) the clock circuit for decreasing a frequency of the first clock signal when the first FCB is for operating in the reduced power consumption mode of operation.

11. A method of controlling power consumption:

providing a first FCB for processing data using a first clock signal provided by a first clock circuit;

providing a second FCB for processing data using a second clock signal provided by a second clock circuit;

receiving a FCB control signal by the first FCB and the second FCB;

determining whether the FCB control signal is for operating of at least one of the first FCB and the second FCB in one of a normal mode of operation and a reduced power consumption mode of operation; and,

performing one of enabling of at least one of the first clock circuit and a second clock circuit in dependence upon whether at least one of the first FCB and the second FCB are for operating in the normal mode of operation and varying a frequency of at least one of the first clock circuit and a second clock circuit in dependence upon whether at least one of the first FCB and the second FCB are for operating in the normal mode of operation.

12. A method according to claim 11, wherein determining comprises determining whether at least one of the first FCB and the second FCB are selected for processing of data.

13. A method according to claim 11, wherein operating in the reduced power consumption mode of operation comprises disabling a majority of internal circuitry within at least one of the first FCB and the second FCB.

14. A method according to claim 11, wherein the first FCB provides a first FCB control signal to the second FCB for enabling and disabling circuit portions of the second FCB.

15. A method according to claim 14, wherein the first FCB control signal is for varying a frequency of the second clock signal for the second FCB.

16. A method according to claim 14, comprising increasing a frequency of the first clock signal where the first FCB is for operating in the normal power consumption mode of operation.

17. A method according to claim 11, comprising decreasing a frequency of the second clock signal when the second FCB is for operating in the reduced power consumption mode of operation.

18. A method according to claim 17, comprising increasing a frequency of the second clock signal when the second FCB is for operating in the normal power consumption mode of operation.

19. A method comprising:

providing a first functional circuit block (FCB) for processing of data using a first clock circuit;

providing a second FCB for processing of data using a second clock circuit; and,

switchably enabling and disabling the first and second clock circuits independently in dependence upon performance requirements of the first and second FCBs.

20. A method according to claim 19, comprising determining whether at least one of the first FCB and the second FCB are for processing of data, where at least one of the first and second clock circuits are disabled when the at least one of the first FCB and the second FCB are other then for processing of data.

21. A storage medium comprising instruction data stored thereon, the instruction data comprising:

first instruction data for providing a first functional circuit block (FCB) for processing of data using a first clock circuit;

second instruction data for providing a second FCB for processing of data using a second clock circuit; and,

third instruction data for switchably enabling and disabling the first and second clock circuits independently in dependence upon performance requirements of the first and second FCBs.

22. A storage medium comprising instruction data stored thereon, the instruction data comprising:

first instruction data for providing a first FCB for processing data using a first clock signal provided by a first clock circuit;

second instruction data for providing a second FCB for processing data using a second clock signal provided by a second clock circuit;

third instruction data for receiving a FCB control signal by the first FCB and the second FCB;

fourth instruction data for determining whether the FCB control signal is for operating of at least one of the first FCB and the second FCB in one of a normal mode of operation and a reduced power consumption mode of operation; and,

fifth instruction data for performing one of enabling of at least one of the first clock circuit and a second clock circuit in dependence upon whether at least one of the first FCB and the second FCB are for operating in the normal mode of operation and varying a frequency of at least one of the first clock circuit and a second clock circuit in

dependence upon whether at least one of the first FCB and the second FCB are for operating in the normal mode of operation.